

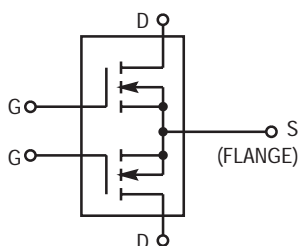
The RF MOSFET Line

RF Power Field-Effect Transistor

N-Channel Enhancement-Mode MOSFET

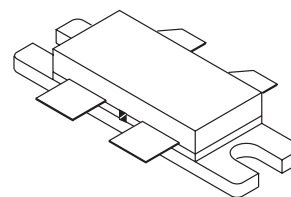
Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 28 V:
Output Power — 300 W
Gain — 12 dB (14 dB Typ)
Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- S-Parameters Available for Download into Frequency Domain Simulators.
See <http://motorola.com/sps/rf/designtds/>



MRF141G

300 W, 28 V, 175 MHz
N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 375-04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage	V_{DGO}	65	Vdc
Gate-Source Voltage	V_{GS}	± 40	Vdc
Drain Current — Continuous	I_D	32	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	500 2.85	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	$^\circ\text{C/W}$

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 100$ mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28$ V, $V_{GS} = 0$)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current ($V_{GS} = 20$ V, $V_{DS} = 0$)	I_{GSS}	—	—	1.0	μAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 100$ mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage ($V_{GS} = 10$ V, $I_D = 10$ A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance ($V_{DS} = 10$ V, $I_D = 5.0$ A)	g_{fs}	5.0	7.0	—	mhos

DYNAMIC CHARACTERISTICS (1)

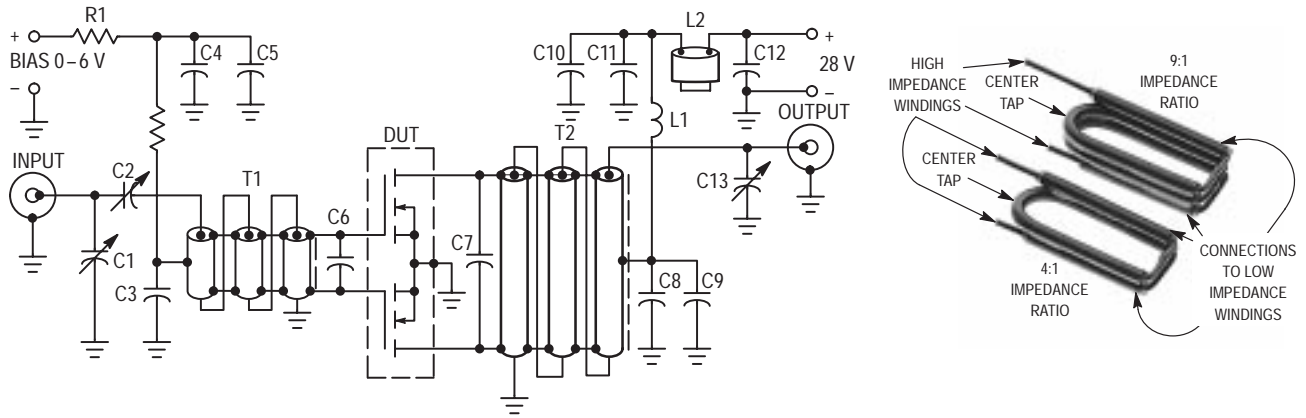
Input Capacitance ($V_{DS} = 28$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	350	—	pF
Output Capacitance ($V_{DS} = 28$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{rss}	—	35	—	pF

FUNCTIONAL TESTS (2)

Common Source Amplifier Power Gain ($V_{DD} = 28$ V, $P_{out} = 300$ W, $I_{DQ} = 500$ mA, $f = 175$ MHz)	G_{ps}	12	14	—	dB
Drain Efficiency ($V_{DD} = 28$ V, $P_{out} = 300$ W, $f = 175$ MHz, I_D (Max) = 21.4 A)	η	45	55	—	%
Load Mismatch ($V_{DD} = 28$ V, $P_{out} = 300$ W, $I_{DQ} = 500$ mA, $f = 175$ MHz, VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:

1. Each side measured separately.
2. Measured in push–pull configuration.



- C1 — Arco 402, 1.5–20 pF
- C2 — Arco 406, 15–115 pF
- C3, C4, C8, C9, C10 — 1000 pF Chip
- C5, C11 — 0.1 μ F Chip
- C6 — 330 pF Chip
- C7 — 200 pF and 180 pF Chips in Parallel
- C12 — 0.47 μ F Ceramic Chip, Kemet 1215 or Equivalent
- C13 — Arco 403, 3.0–35 pF
- L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4" I.D.
- L2 — Ferrite Beads of Suitable Material for 1.5–2.0 μ H Total Inductance
- R1 — 100 Ohms, 1/2 W
- R2 — 1.0 kOhm, 1/2 W

- T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co-Ax, 62–90 Mils O.D.
- T2 — 1:9 RF Transformer. Can be made of 15–18 Ohms Semirigid Co-Ax, 70–90 Mils O.D.

Board Material — 0.062" Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, $\epsilon_r = 5$

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See pictures for construction details.

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

Figure 1. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

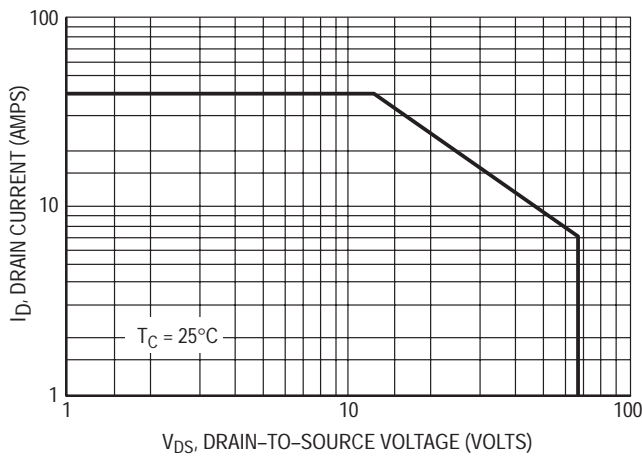


Figure 2. DC Safe Operating Area

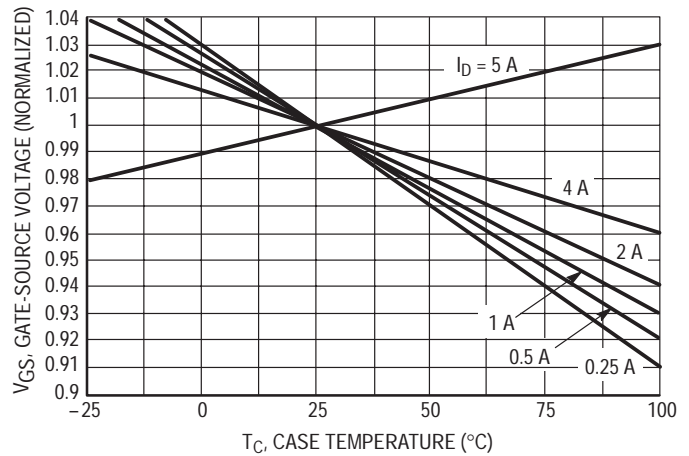
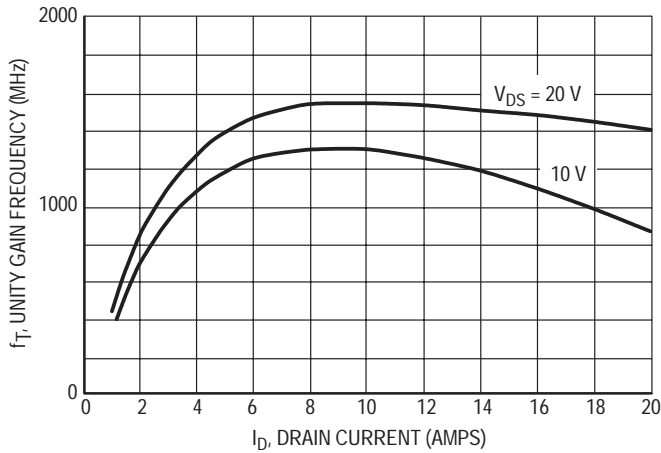


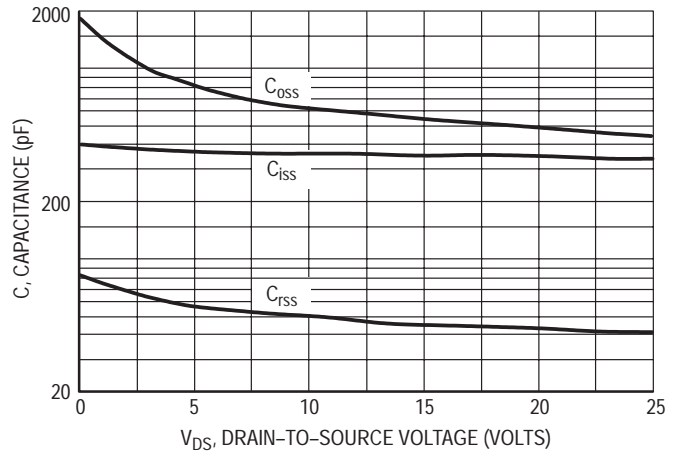
Figure 3. Gate-Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS



NOTE: Data shown applies to each half of MRF141G.

Figure 4. Common Source Unity Gain Frequency versus Drain Current



NOTE: Data shown applies to each half of MRF141G.

Figure 5. Capacitance versus Drain-Source Voltage

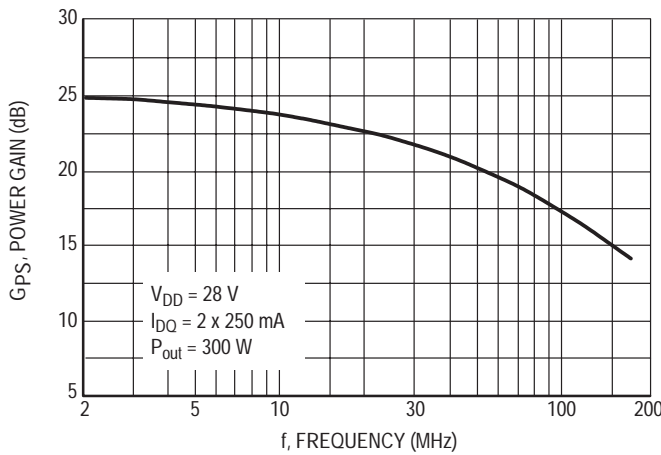


Figure 6. Power Gain versus Frequency

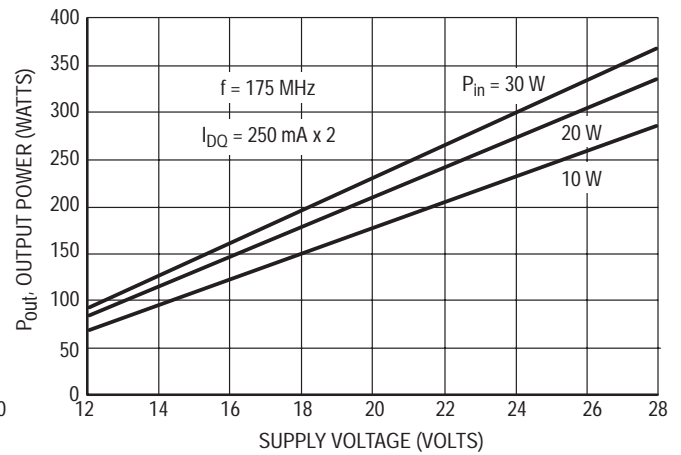
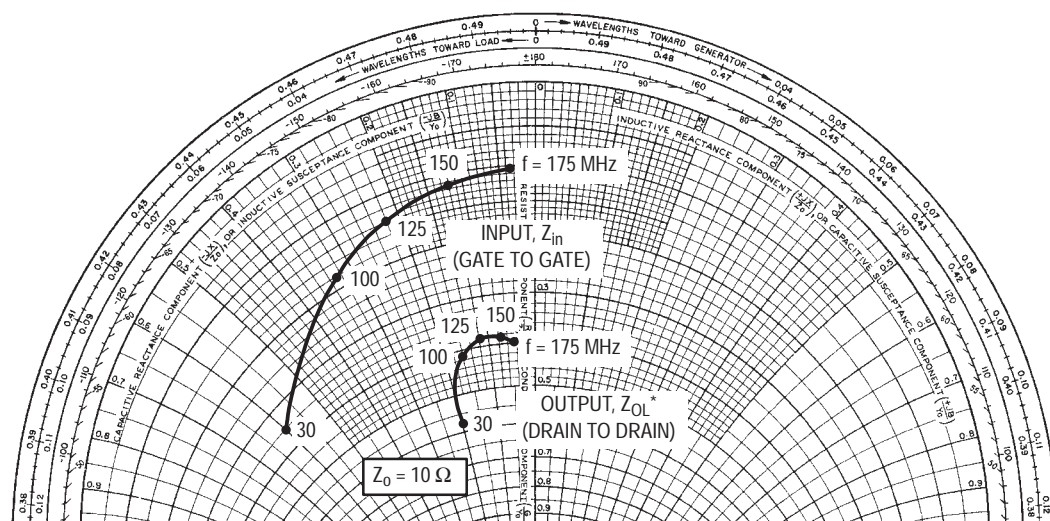


Figure 7. Output Power versus Supply Voltage



Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 8. Input and Output Impedances

NOTE: S-Parameter data represents measurements taken from one chip only.

Table 1. Common Source S-Parameters ($V_{DS} = 24\text{ V}$, $I_D = 0.57\text{ A}$)

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
30	0.845	-174	4.88	78	0.014	-5	0.939	-174
40	0.867	-174	3.23	66	0.013	-14	0.856	-172
50	0.876	-174	2.62	62	0.013	-17	0.868	-175
60	0.883	-174	2.12	59	0.012	-15	0.938	-176
70	0.890	-175	1.85	58	0.012	-12	1.036	-177
80	0.899	-175	1.57	56	0.011	-10	1.110	-177
90	0.909	-175	1.36	50	0.010	-11	1.190	-176
100	0.920	-176	1.13	43	0.009	-13	1.160	-176
110	0.930	-176	0.95	37	0.007	-16	1.100	-177
120	0.938	-176	0.78	33	0.007	-11	1.010	-175
130	0.944	-176	0.67	31	0.006	-3	0.954	-176
140	0.948	-177	0.60	31	0.006	10	0.964	-177
150	0.951	-177	0.56	32	0.005	23	1.023	-178
160	0.954	-178	0.52	32	0.005	31	1.130	-179
170	0.958	-178	0.48	29	0.006	37	1.190	-178
180	0.962	-178	0.45	24	0.006	39	1.260	-179
190	0.965	-179	0.40	17	0.007	41	1.200	180
200	0.968	-179	0.34	15	0.008	49	1.090	-179
210	0.970	-179	0.30	15	0.008	60	0.980	-178
220	0.972	-180	0.27	15	0.008	68	0.960	-177
230	0.973	-180	0.25	17	0.008	68	1.045	-179
240	0.974	180	0.24	20	0.009	67	1.030	179
250	0.975	180	0.24	19	0.011	68	1.100	179
260	0.977	179	0.21	17	0.012	69	1.200	179
270	0.978	179	0.22	13	0.013	72	1.210	177
280	0.979	179	0.19	13	0.012	72	1.170	177
290	0.979	178	0.17	1	0.012	68	1.040	180
300	0.980	178	0.16	8	0.013	65	0.998	179
310	0.980	178	0.16	13	0.015	70	0.977	179
320	0.981	178	0.16	15	0.017	76	0.979	178
330	0.982	177	0.13	10	0.017	83	1.033	178
340	0.982	177	0.15	19	0.016	81	1.110	176
350	0.982	177	0.13	16	0.016	73	1.140	177
360	0.983	177	0.13	8	0.020	63	1.150	177
370	0.982	176	0.10	6	0.023	65	1.120	176
380	0.982	176	0.10	7	0.023	72	1.050	177
390	0.982	176	0.10	10	0.021	81	0.993	177
400	0.982	176	0.09	14	0.018	83	0.959	179
410	0.983	175	0.10	12	0.020	71	1.040	176
420	0.983	175	0.09	16	0.025	65	1.090	174
430	0.984	175	0.09	15	0.028	70	1.100	174

Table 1. Common Source S-Parameters ($V_{DS} = 24\text{ V}$, $I_D = 0.57\text{ A}$) continued

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
440	0.983	174	0.09	12	0.028	77	1.100	175
450	0.983	174	0.09	13	0.025	82	1.090	176
460	0.983	174	0.07	14	0.022	66	1.080	174
470	0.983	174	0.07	13	0.024	56	0.992	175
480	0.983	174	0.07	16	0.032	60	0.970	175
490	0.984	173	0.07	13	0.036	74	0.996	174
500	0.984	173	0.07	18	0.035	85	1.040	174

Table 2. Common Source S-Parameters ($V_{DS} = 28\text{ V}$, $I_D = 0.65\text{ A}$)

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
30	0.849	-174	5.41	79	0.013	-6	0.934	-174
40	0.869	-174	3.59	67	0.013	-16	0.849	-172
50	0.878	-174	2.91	62	0.012	-17	0.859	-174
60	0.884	-174	2.36	60	0.011	-13	0.928	-176
70	0.890	-175	2.06	59	0.010	-11	1.029	-177
80	0.899	-175	1.75	56	0.009	-14	1.110	-177
90	0.910	-176	1.52	51	0.009	-18	1.190	-175
100	0.920	-176	1.26	43	0.009	-19	1.150	-175
110	0.929	-176	1.07	37	0.008	-15	1.100	-177
120	0.937	-176	0.88	34	0.006	-4	1.000	-175
130	0.943	-176	0.75	32	0.004	5	0.953	-176
140	0.947	-177	0.67	32	0.003	6	0.966	-177
150	0.950	-177	0.63	32	0.004	6	1.030	-178
160	0.953	-178	0.58	32	0.005	18	1.120	-178
170	0.957	-178	0.54	29	0.006	36	1.180	-178
180	0.961	-178	0.51	24	0.006	53	1.250	-179
190	0.964	-179	0.45	18	0.006	65	1.200	180
200	0.967	-179	0.39	15	0.005	69	1.110	-179
210	0.969	-179	0.35	15	0.005	63	1.030	-178
220	0.971	-180	0.31	15	0.006	59	0.975	-177
230	0.972	-180	0.28	17	0.009	66	1.040	-179
240	0.973	180	0.27	20	0.010	78	1.030	179
250	0.974	180	0.27	19	0.010	88	1.090	180
260	0.976	179	0.24	17	0.009	85	1.200	179
270	0.977	179	0.24	12	0.010	73	1.220	177
280	0.978	179	0.21	12	0.011	66	1.170	178
290	0.979	178	0.19	2	0.013	70	1.040	180
300	0.979	178	0.18	8	0.013	78	1.000	179
310	0.979	178	0.17	13	0.013	89	0.975	179
320	0.980	178	0.17	14	0.012	88	0.988	177
330	0.981	177	0.14	9	0.013	80	1.050	177
340	0.982	177	0.16	17	0.015	75	1.110	176

Table 2. Common Source S-Parameters ($V_{DS} = 28\text{ V}$, $I_D = 0.65\text{ A}$) continued

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
350	0.982	177	0.15	14	0.018	80	1.130	177
360	0.982	177	0.14	8	0.018	82	1.160	177
370	0.982	176	0.12	6	0.017	82	1.120	176
380	0.982	176	0.12	6	0.015	77	1.060	177
390	0.982	176	0.11	9	0.016	72	0.992	177
400	0.982	176	0.10	13	0.018	78	0.958	179
410	0.983	175	0.11	11	0.021	83	1.050	176
420	0.983	175	0.10	15	0.021	87	1.070	175
430	0.983	175	0.10	14	0.019	85	1.090	175
440	0.983	174	0.10	10	0.018	76	1.130	175
450	0.983	174	0.10	9	0.021	71	1.130	176
460	0.982	174	0.08	10	0.024	70	1.080	174
470	0.983	174	0.08	11	0.023	82	0.996	175
480	0.983	174	0.08	15	0.021	90	0.974	176
490	0.983	173	0.08	12	0.019	87	0.971	175
500	0.983	173	0.08	17	0.021	78	1.010	174

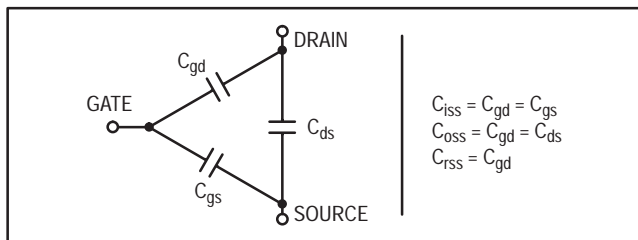
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially a capacitor. Circuits that leave the gate open-circuited or float-

ing should be avoided. These conditions can result in turn-on of the device due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF141G is an RF Power, MOS, N-channel enhancement mode field-effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

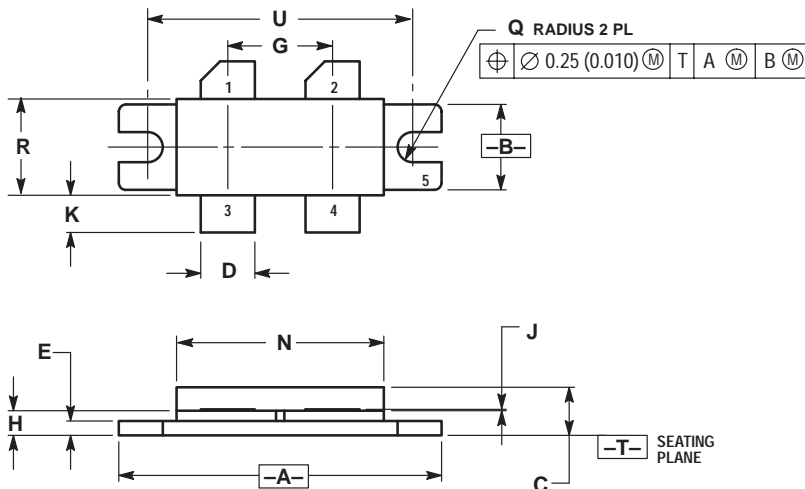
The MRF141G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF141G was characterized at $I_{DQ} = 250$ mA, each side, which is the suggested minimum value of I_{DQ} . For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF141G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

- STYLE 2:
 PIN 1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

CASE 375-04 ISSUE D

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